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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	18

Application Number	09/912,806
Filing Date	July 24, 2001
First Named Inventor	BIRGER GERNHARDT
Art Unit	2114
Examiner Name	Anne L. Damiano
Attorney Docket Number	7031 US

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  Appendix
  Return Post Card

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	TEKTRONIX, INC.		
Signature	Francis I. Gray		
Printed name	FRANCIS I. GRAY		
Date	JANUARY 4, 2005	Reg. No.	27,788

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Pauline L. Bradley		
Typed or printed name	Pauline L. Bradley	Date	JANUARY 4, 2005

PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 20-0352 Deposit Account Name: TEKTRONIX, INC.

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 20 or HP =	_____	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 3 or HP =	_____	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof	Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____ (round up to a whole number)	x _____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): APPEAL BRIEF	500.00

SUBMITTED BY

Signature	Francis I. Gray	Registration No. (Attorney/Agent) 27,788	Telephone 503 627-7261
Name (Print/Type)	FRANCIS I. GRAY		Date JANUARY 4, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **BIRGER GERNHARDT**

Filed: **July 24, 2001**

Examiner: **Anne L. Damiano**

Serial No.: **09/912,806**

Art Unit: **2114**

For: **DEVICE FOR ANALYZING DIGITAL DATA**

January 4, 2005

Mail Stop Appeal Brief - Patents
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APPEAL BRIEF

Dear Sir:

This is an appeal from the final rejection by the Examiner of claims 1-13, the only claims in the case, over prior art.

Real Party in Interest

The real party in interest is Appellant's assignee, Tektronix International Sales Gmbh of Schauffhausen, Switzerland.

Related Appeals and Interferences

There are no related appeals and interferences known to Appellant, Apellant's legal representative or Appellant's assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1 and 3-8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Dorsey et al ("Dorsey" U.S. Patent No. 6,198,751), and claims 2 and 4-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey. Claims 1-13 are the subject of this appeal.

Status of Amendments

No amendments were filed subsequent to the Examiner's final rejection.

Summary of Invention

The present invention is a device (Fig. 2) for analyzing digital data formulated in accordance with a communication protocol, the device having a data memory 26 for storing the digital data 25 to be analyzed and a microcode memory 18 for storing a microprogram 20 that contains information in the form of a tree of rules on at least part of one communication protocol to be decoded. (Page 4, lines 11-17) Data is read from the data memory as addressed by a data addressing unit 34 for transfer to a data register 28, and microcode is read from the microcode memory as addressed by a microcode addressing unit 40 for transfer to a microcode register 22. A register block 36 has inputs from the data register and the microcode register, and provides input to the respective addressing units. The microcode addressing units also have inputs from the data register and the microcode register, while the data addressing

unit has an input from the microcode addressing unit. Data from the data register and the microcode register are input via a multiplexer 52 to an output memory 30 that has its own addressing unit 46 with an input from the microcode register. A logic unit 50 combines input from the output memory and the microcode register to provide another input to the multiplexer 52. The register block has several registers and counters, the contents of which impact subsequent addresses in the data and/or microcode memories. (Page 5, line 3 - page 6, line 3) The content of the data register represents a pre-determined number of bits from the data memory, and the content of the microcode register is used for analyzing the content of the data register.

The start of a decoding process is initiated via a "Start" signal 44 to the microcode addressing unit, which causes starting addresses 38, 42, 48 to be loaded into both the data and microcode addressing units, and maybe the output addressing unit. In this way the device becomes aware of the address in the data memory at which data analysis is to start and where entry into the stored microcode occurs. The respective data/microcode are read into the respective registers and the data are assigned functions according to the microcode section in the microcode register – PDU (Protocol Data Unit) type, parameter identification (ID), parameter value, etc. Analysis results are entered into the output memory, and results that might have an effect on subsequent addresses are entered in the register block, which affects the next addresses accordingly. (Page 7, line 13 - page 8, line 14; Fig. 3) When there is a new result, prior entries are read from the output memory, linked with the new result, and re-entered into the output memory. (Page 8, lines 17-19) If a PDU extends across several addresses and the parameter searched for has

already been found, it is possible from the length of the relevant PDU filed in the register block to jump directly to the next address of interest which indicates the beginning of the next PDU, rather than traverse addresses sequentially. (Page 9, lines 16-22)

Issues

1) Whether claims 1 and 3-8 are anticipated by Dorsey under 35 U.S.C. 102(e)?

2) Whether claims 2 and 4-13 are obvious to one of ordinary skill in the art in view of Dorsey under 35 U.S.C. 103(a)?

Grouping of Claims

Claims 1, 2, 4, 6, 8, 10, 12 and 13 are deemed to be independently patentable. Claims 3, 5, 7, 9 and 11 are deemed to stand or fall together with the claims from which they depend.

Argument

1. Anticipation of claims 1 and 3-8 by Dorsey

35 U.S.C. 102(e) provides in pertinent part that a "person shall be entitled to a patent unless – (e) invention was described in . . . a patent granted on an application

for patent by another filed in the United States before the invention by the applicant for patent." Generally in order to be anticipatory all the elements of the claim must be found within the four corners of a single prior art patent.

In contradistinction to Appellant's claimed invention Dorsey discloses a Multi-protocol Packet Translator (MPT) for translating information packets from one network protocol to another network protocol. Each received packet is received in an input memory 21a and a controller 24 determines what translation is required. The translation process is performed by two elements – the MPT 26 and a direct memory access (DMA) controller 27. The MPT translates the header and trailer information from the first protocol into the header and trailer information for the new packet in a second protocol for storage in an output memory 21b. The MPT may also pass the data through where useful when the trailer or other field is based on the contents of the entire packet, otherwise the data is transferred by the DMA directly from the input memory to the output memory. An address control unit 53b controls what memory location is read from the input memory for use in the translation, and the MPT includes FIFOs 54, 55 where new header/trailer information is stored as required for the translation, i.e, to replace or supplement the original header/trailer information during the translation. A multiplexer 56 selects between the input memory output and the FIFO outputs for input to the output memory. A translator control unit 59 is microcoded, and includes an opcode memory 51a that stores various instructions required for all translations that might be performed, with an address control unit 51b controlling which instructions are stepped through for performance. The instructions are input to a pipeline unit 52 implemented as a three-stage, two-register pipeline, with one register used for

opcodes from the opcode memory and the other used for operands from the opcode memory. At the start of translation the controller selects the appropriate instruction set from the opcode memory for use and sets the opcode address control unit to the appropriate start location for the translation. Controller 50 takes the opcode information from the pipeline and sends control signals to the information sources and the multiplexer. Note that the address control units are clocked, i.e., the addresses are stepped through so once the translation process starts there are no address jumps.

Claim 1

The Examiner takes the position that Dorsey discloses a device for analyzing digital data formulated in accordance with a communication protocol, whereas the title and description in Dorsey describe a Multi-protocol Packet Translator (MPT) that takes the heads and tails of an input protocol message and converts them into heads and tails of an output protocol message. The Examiner equates the claimed data memory for storing digital data to be analyzed with the input memory 21a of Dorsey, stating that the data to be translated is analyzed in the translation process, although Dorsey does not indicate any "analysis" occurring. The Examiner then equates the claimed microcode memory for storing a microcode that represents at least part of the communication protocol with the controller 50 of Dorsey, referring to a memory 51a that is loaded with sets of microcode instructions, each set being designed to perform a particular network communication protocol translation – not analysis. The Examiner goes on to equate the claimed data register for reading out

a pre-determined number of bits from the data memory by stating that, when the packet in the data memory of Dorsey is translated, it's content will be loaded to a register in the translator control unit 59, apparently referencing the pipeline unit 52 that deals with opcodes and operands -- not with data from the input data memory. Then the Examiner equates the claimed microcode register for reading out a pre-determined number of bits from the microcode memory, with the content of the microcode register being usable for analyzing the content of the data register reference, to the selection of the particular set of microcodes required for a particular translation, not to a subset of microcode that is required for analyzing the data in the data register. The Examiner further equates the output memory into which the results of the analysis are entered with the output memory 21b where the translated packets are stored, which are not analysis results. The Examiner also equates the first addressing unit for addressing the data memory with the address control 53b for the input memory of Dorsey. Finally the Examiner equates the second addressing unit for addressing the microcode memory with the address control 51b for the obcode memory of Dorsey, referencing the selecting of the appropriate set of microcode required for the particular translation, referencing the controller setting a start address in the address control for the start of the translation process, i.e., selecting the set of mirocode for the translation. Appellant recites that the first and second addressing units are designed to take into account the content of the data register and/or microcode register when subsequent addresses are determined, and the Examiner states that the addressing units of Dorsey control the writing to the output memory (which this claimed element does not address) including its associated address control by taking into account the content of the input memory

(not the data register) and the microcode translation instructions (not the microcode in the microcode register) and that, since the process occurs sequentially, the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcode memory. Appellant fails to see how writing to the output memory in Dorsey has anything to do with how the subsequent addresses for the data and/or microcode memories are determined, i.e., from the content of the data and/or microcode registers as recited in the claim.

Putting Dorsey in its best light, Appellant submits that Dorsey may show an input memory with address control unit, an output memory with address control unit, an opcode memory with address control unit, and a multiplexer that selects input from information sources and the opcode memory. The pipeline registers may even arguably be equated to Appellant's microcode register. However Appellant submits that Dorsey neither teaches nor suggests the respective data and microcode registers so that only a part of the protocol is processed at any one time, nor does Dorsey teach or suggest that the addressing units receive inputs from any data/microcode registers as is recited in claim 1. Thus claim 1 is deemed to be neither anticipated nor rendered obvious to one of ordinary skill in the art by Dorsey since Dorsey does not disclose all the elements recited by Appellant and does not disclose the elements operating with each other as recited by Appellant.

Claim 4

The Examiner states that Dorsey discloses a device having a register block, referencing the output address control for the output memory 58, with at least one

register and at least one counter (clock), the contents of which are taken into account for determining the subsequent addresses for the first and second address units taking into account the contents of the data and/or microcode registers. As pointed out above, Dorsey does not have a data register; the noted address control does not have access to the data/microcode registers and so cannot take them into account; and the noted address control has no interaction at all with the input and opcode address controls and so cannot determine the addresses for such address controls. The section at column 8 cited by the Examiner deals with how the opcode instructions are processed. Further the Examiner refers to the address units as controlling the writing to the output memory including its associated address control, and since this process occurs sequentially the address to which the data is written in the output memory is subsequent to the addresses of the data memory and microcode memory. Since this element has nothing to do with writing into the output memory, Appellant fails to see its pertinence. The claimed register block is coupled to the data and microcode registers ("take into account the contents of the data register and/or the microcode register") and affects the addresses in the data and microcode addressing units ("determining the subsequent addresses for the first and second addressing units"). Since the Examiner's argument deals with writing to the output memory, and the cited element in claim 4 does not deal with the output memory, Appellant submits that claim 4 is neither anticipated nor rendered obvious to one of ordinary skill in the art by Dorsey.

Claim 6

The Examiner states that column 8, lines 24-31 of Dorsey (controller [50] controls the multiplexer which selects the data fed to the output memory, and controls the output memory including its associated address control) equates to the claimed "logic circuit with which an entry into the output memory is read out, changed to take into account a new result, and rewritten into the output memory." Appellant fails to see any indication that Dorsey reads out an entry that is in the output memory, changes it and then rewrites it to the memory. Therefore Dorsey neither teaches or suggests to one of ordinary skill in the art this logic circuit for performing a read/modify/write operation. Thus claim 6 is neither anticipated nor rendered obvious by Dorsey.

Claim 8

The Examiner states that the translated header includes information identifying the network protocol, and states that this is equivalent to parameters. Claim 8 recites that "the digital data to be analyzed are protocol data units that contain parameters, and the results entered into the output memory have at least one parameter identifier and at least one parameter value." Appellant submits that header translation from one protocol to another is not equivalent to analyzing PDUs to produce results that include an ID and value. Thus claim 8 is deemed to be neither anticipated nor rendered obvious to one of ordinary skill in the art by Dorsey.

In view of the above discussion claims 1 and 3-8 are deemed to be allowable as being neither anticipated nor rendered obvious by Dorsey.

2. Obviousness of claims 2 and 4-13 in view of Dorsey

Claim 2

The Examiner states that Dorsey does not disclose each addressing unit has a counter that may be changed in accordance with the content of the data register and/or microcode register when the subsequent addresses are determined, but concludes that is would have been obvious that Dorsey's address units have address counters that change in accordance with the content of the data registers. However in fact there is no teaching or suggestion that the address control units of Dorsey are controlled by data content, especially since Dorsey (as pointed out above) does not have any data registers. Therefore claim 2 is nonobvious to one of ordinary skill in the art over Dorsey.

Claims 4, 6 and 8

As pointed out above Dorsey does not really teach or suggest a register block as recited by Appellant, and merely reiterates here the same argument made above with respect to claim 4. Likewise the Examiner makes the same arguments as above with regards to claims 6 and 8. For the reasons expressed above claims 4, 6 and 8 are nonobvious to one of ordinary skill in the art over Dorsey.

Claim 10

This claim is comparable to claim 1, but in a method claim format. The Examiner reiterates the same arguments as above. Here the Examiner admits that Dorsey does not specifically disclose updating counter reading for the first and second addressing units in accordance with the contents of the data register (which Dorsey does NOT have) and/or the microcode register, but asserts it would have been obvious to have address counters that change in accordance with the content of the data registers. For the same reasons recited to rebut the Examiner's rejection of claim 1, claim 10 is deemed to be allowable as being nonobvious to one of ordinary skill in the art over Dorsey.

Claim 12

For the reasons discussed above with respect to claim 6, claim 12 is deemed to be allowable as being nonobvious to one of ordinary skill in the art over Dorsey.

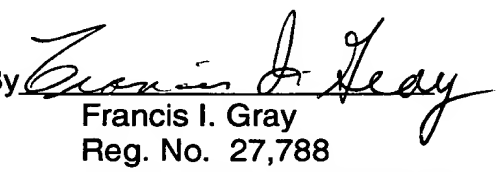
Claim 13

For the reasons discussed above with respect to claim 4, claim 13 is deemed to be allowable as being nonobvious to one of ordinary skill in the art over Dorsey.

In conclusion Appellant requests that the Examiner's rejection of claims 1-13 over Dorsey be reversed, and that this case be passed to issue.

Respectfully submitted,

BIRGER GERNHARDT

By 
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APPENDIX

Appealed Claims

1. A device for analyzing digital data formulated in accordance with a communication protocol, comprising:

a. a data memory for storing the digital data to be analyzed;

b. a microcode memory for storing a microcode that represents at least part of the communication protocol;

c. a data register for reading out a pre-determined number of bits from the data memory;

d. a microcode register for reading out a pre-determined number of bits from the microcode memory, with the content of the microcode register being usable for analyzing the content of the data register;

e. an output memory into which the results of the analysis are entered;

f. a first addressing unit for addressing the data memory; and

g. a second addressing unit for addressing the microcode memory, with the first and second addressing units being designed to take into account the content of the data register and/or the microcode register when subsequent addresses are determined.

2. The device according to claim 1 wherein the first and second addressing units each comprise at least one counter that may be changed in accordance with the content of the data register and/or microcode register when the subsequent addresses are determined.

3. The device according claim 1 wherein the data register is designed to align and/or shift its content.

4. The device according to claims 1, 2 or 3 further comprising a register block with at least one register and at least one counter, the contents of which are taken into account for determining the subsequent addresses for the first and second addressing units, the at least one register and the at least one counter being used to take into account the contents of the data register and/or the microcode register.

5. The device according to claim 4 further comprising a third addressing unit for the output memory, with the address of the third addressing unit being changeable by taking the content of the microcode register into account.

6. The device according to claim 5 further comprising a logic circuit with which an entry into the output memory is read out, changed to take into account a new result, and rewritten into the output memory.

7. The device according to claim 6 wherein a starting address is loaded into the addressing units.

8. The device according to claim 7 where the digital data to be analyzed are protocol data units that contain parameters, and the results entered into the output memory have at least one parameter identifier and at least one parameter value.

9. The device according to claim 8 wherein at least two of the memories are combined in one physical memory, and the corresponding addressing units are combined in one physical addressing unit.

10. A method of analyzing digital data formulated in accordance with a communication protocol comprising the steps of:

a. loading the digital data to be analyzed into a data memory;

b. loading a microcode into a microcode memory, with the microcode representing at least part of the communication protocol;

c. reading out a pre-determined number of bits from the data memory into a data register in accordance with an address specified by a first addressing unit;

d. reading out a pre-determined number of bits from the microcode memory into a microcode register in accordance with an address specified by a second addressing unit;

e. assigning functions to the data bits in the data register according to the microcode bits in the microcode register;

f. entering at least one result of the assignment in an output memory; and

g. updating counter readings for the first and second addressing units in accordance with the content of the data register and/or the microcode register.

11. The method according to claim 10 wherein the entry in accordance with step f) takes place at an address specified by a third addressing unit, with a counter reading for the third addressing unit being updated in accordance with the content of the microcode register.

12. The method according to claim 11 wherein prior to entry in accordance with step f) an incomplete entry is read out from the output memory by a logic circuit and changed to take into account a new result, and then rewritten into the output memory.

13. The method according to claims 10, 11 or 12 comprising in a further step a register block containing at least one register and at least one counter which is loaded with the results of the analysis and which are taken into account when subsequent addresses are determined for the first and second addressing units.